

KL5BUDV003 LSI Data Sheet (abridged edition)

Rev 1.0

Kawasaki Microelectronics, Inc.

Kawasaki LSI, Inc.

Revision History

History	Date	Update information
0.1	2/12/2002	First Draft
1.0	7/26/2002	

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1. Overview of Product

The KL5BUDV003 LSI is the new version of Kawasaki's USB product. It is designed based on KL5BUDV002 (U2PCI) and added new feature. The major improvement is as followings.

1. Include USB2.0 transceiver.
2. Multiple the endpoint.
3. Add IHOST interface

The followings are the summary of the chip feature.

1. USB2.0 PHY and USB to PCI function are integrated with Kawasaki's KS6000 0.18um standard cell technology
2. PCI bus of 33MHz and 32bit is supported
3. Up to 4 DMACs are supported for PCI master operation.
4. Two DMA memory access methods are available for PCI master operation.
5. Up to 5 endpoints are supported for USB high speed and full speed operation.
6. 33MHz PCI clock and 48MHz USB clock are used for operation
7. High performance of using double buffering and internal DMA operation.
8. IHOST interface for the CPU incapable of PCI .
9. Low power device such as typical 120mA for 2 endpoints DMA operation and 150mA for 5 endpoints DMA operation (preliminary value).
10. operation voltage I/O and analog:3.3V \pm 0.3 V, Core : 1.8V \pm 0.15V
11. ambient temperature 0 to 70 C
12. LQFP144 package (20mm-sq)

2. Overview of Functions

2.1. Chip Features

KL5BUDV003 consists of USB201IP (USB2.0 transceiver function), HS_SIE, 4 sets of DBUF (Data buffer of 512Bytes x 2 for USB high speed operation and 64Bytes x 2 for USB full speed operation), U2PCTRL, which includes PCI configuration registers and PCI interface including 6 PCI DMAC). Chip can perform around 400Mb/s throughput in ideal situation - no wait cycle is in both USB and PCI bus - from simulation result. Major chip

functionality is as follows.

USB2.0 High Speed Transceiver

Include USB2.0 High Speed buffer and analog interface. Also the digital serial bit processing are encapsulated.

HS_SIE feature (also supporting FS)

Capable of HS chirp protocol and HS/FS judgement.

Performs basic level USB operation and basic transaction flow control.

Up to 5 endpoints supported

Endpoint 0	Control Transfer	64-byte buffer
Endpoint 1	Bulk OUT	512-byte x2 buffer
Endpoint 2	Bulk IN	512-byte x2 buffer
Endpoint 3	Bulk OUT	512-byte x2 buffer
Endpoint 4	Bulk IN	512-byte x2 buffer
Endpoint 5	Interrupt IN	8-byte buffer

PCI bus IF

Pin configuration based on installation on PCI bus – 33 MHz, 32 bit, side B

Target single access - Internal register access (memory mapped)

Master burst access (two DMA modes selectable by register)

- DMAC_P(page) mode: Access external 4kByte page in PCI master mode. Page access information is located in the device, while page table is stored in external memory.
- DMAC_D(descriptor) mode: Access external 4, 16, 32 or 64 kByte memory block in PCI master mode. Block access information is located in descriptor chain in external memory. Block size is selectable during initialize.

IHOST bus IF

16bits bus with register access and 4-channel DMA. The register access mode needs only HCSN, HWRN, HRDN and HRDY for control.

DMA access is controled with HREQ and HACK signal. Each 4-channel DMA has independent control signals.

2.2. Correspondence endpoints to DMAC

In DMAC_D mode, PCI RD and WR can operate in time-division, and also the endpoints can be selected independently. The following table is the summary of the operation mode of DMAC_D.

Table 2.2.1. Operation mode of DMAC_D

Op.-mode															
DMAC_D1(WR) Endpoint1(BO)	X		X				X		X	X		X	X		X
DMAC_D2(RD) Endpoint2(BI)		X	X					X	X		X	X		X	X
DMAC_D3(WR) Endpoint3(BO)				X		X	X	X	X				X	X	X
DMAC_D4(RD) Endpoint4(BI)					X	X				X	X	X	X	X	X

The shading area is same mode as KL5BUDV002(U2PCI).

In DMAC_P mode, RD and WR mode can't be selected at the same time.

The following table is the summary of the operation mode of DMAC_P.

Table 2.2.2. Operation mode of DMAC_P

Op.-mode								
DMAC_P1(WR) Endpoint1(BO)	X				X	X		
DMAC_P1(RD) Endpoint2(BI)		X					X	X
DMAC_P2(WR) Endpoint3(BO)			X		X		X	
DMAC_P2(RD) Endpoint4(BI)				X		X		X

Note: An internal flag is used to specify the PCI's RD or WR operations. The PCI RD/WR time-division operation in DMAC_D mode employs the round-robin method.

Note: The P_MODE pin and registers can be used to select the master burst length.

P_MODE[2]= =1: Selection by register (4/8/32/64/128/256 bytes)

In this case, MIN_GNT and MAX_LAT in the PCI Config header information are both 0.

P_MODE[2]= =0: Selection by pin P_MODE[1:0] (32/64/128/256 bytes)

MIN_GNT and MAX_LAT are set to predefined values on the basis of a throughput of 400 Mb/s and length information. (Determined when the power is turned on).

Endian switching during DMA data transfer with PCI bus

The Config header and internal registers (other than ones for data transfer) are set to Little Endian. During USB data transfer, Endian can be switched to Big End by internal register settings.

Internal data buffer has a double-buffer configuration that provides independent send and receive buffers.

Buffering is in units of 512 bytes (or a smaller data-transfer unit). The buffer size is 512 bytes (128 DW x 32 bits) x 2 for both USB BO/BI.

Data Integrity

Data is protected in the device even if the PCI or USB host is busy, resulting in interruption of data transfer.

USB configuration

The auto_configuration corresponding to vendor-specific class of our own is provided. The configuration can also be controlled from outside the PCI (default).

Max throughput

Target max throuput is 400 Mb/s if there is no delay factor both the USB and PCI buses .

3. Internal Blocks

3.1. USB201IP block

USB2.0 transceiver phy function is performed in this block. USB transaction lower protocol is processed here. USB201 IP is fully compatible with KL5KUSB201 LSI.

3.2. HS_SIE block

This block controls USB201 IP and also performs upper part of USB device protocol such as packet generation and retry handling. It also has double buffer for each bulk transfer and buffers for control and interrupt transfer.

3.3. DBUF block

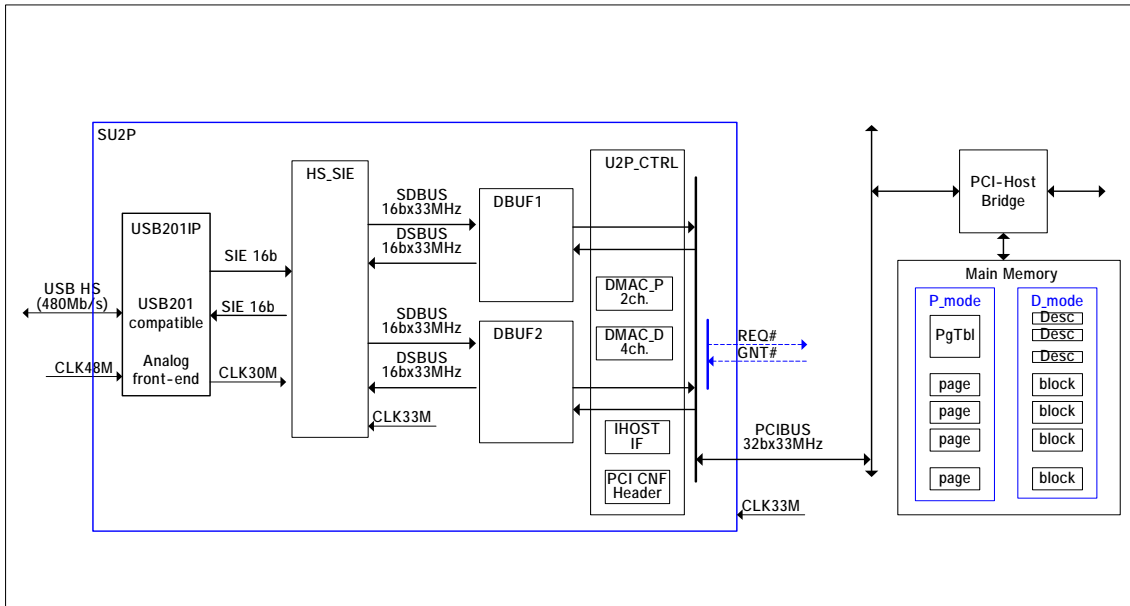
This block handles USB data buffering under the control of the HS_SIE and U2P_CTRL blocks. The block employs a double-buffer configuration that provides independent send buffer (512 bytes x 2) and receive buffer (512 bytes x 2).

3.4. U2P_CTRL block

This block controls the entire device chip and transfers DMA data between the DBUF and external memory using the built-in DMAC_P RD or WR, DMAC_D RD, and DMAC_D WR controllers. This block also contains PCI configuration registers and PCI interface function.

IHOST interface is included in this block. 16bits data transfer is performed by this interface.

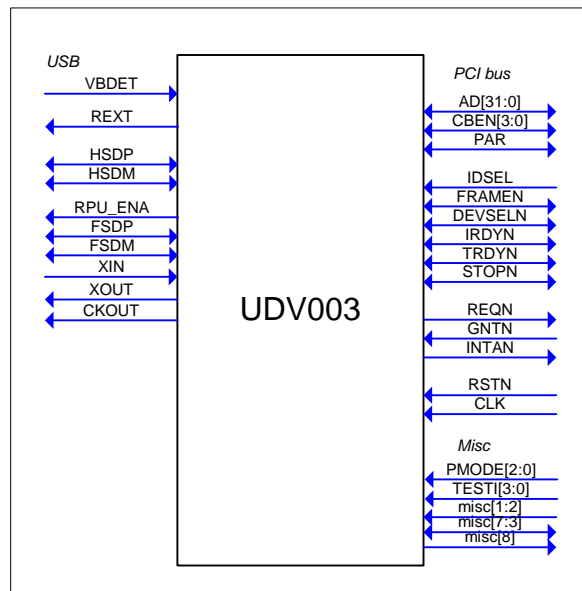
Figure 3. Internal block diagram



4. Logical Pin Out

Figure 4 is the logical pinout. In this figure, only the PCI interface signals are described. About the IHOST interface signals, please refer to section 6.2, signal description.

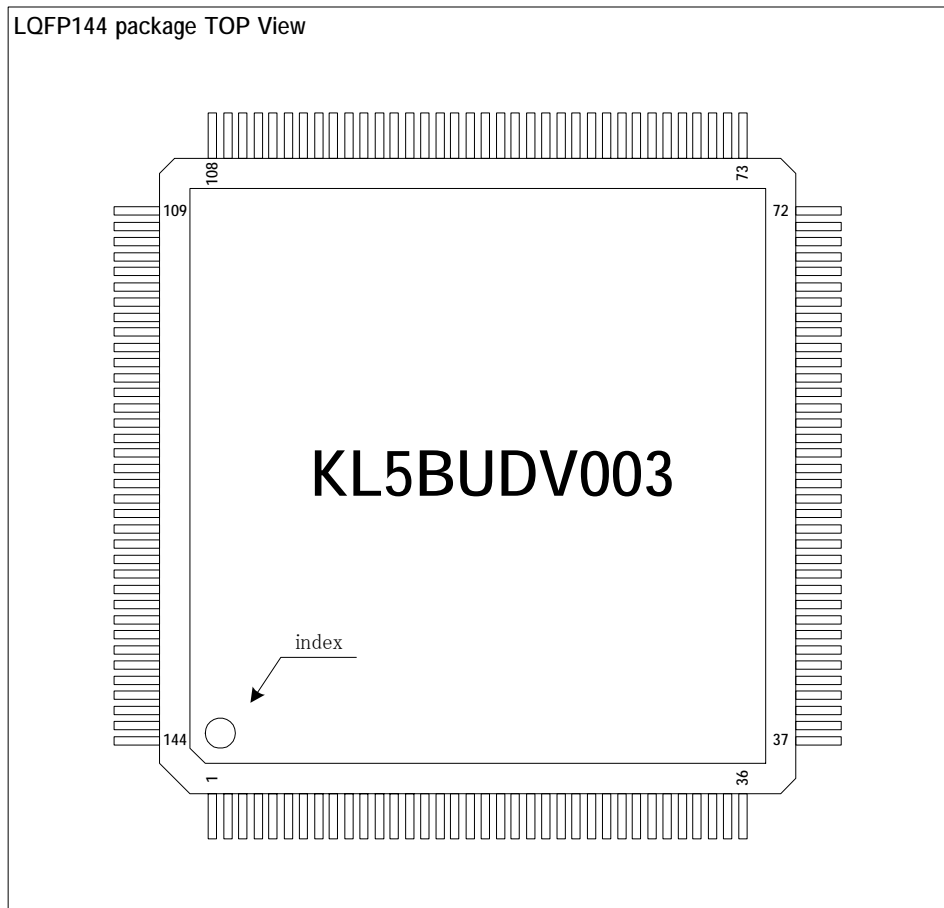
Figure 4 Logical pinout



5. Package Information

The figure 5 is the information of the LQFP144 package.

Figure 5 LQFP144 Package



6. Pin Information

6.1. Pin table

Table 6.1. are pin tables used at PCI mode.

Table 6.1. pin table (PCI mode)

Pin	Signal name	I/O	Bus	Remarks	Pin	Signal name	I/O	Bus	Remarks
1	P_MODE[0]	I	misc	H/L	37	GND		--	gnd
2	P_MODE[1]	I	misc	H/L	38	AD[31]	I/O	PCI	--
3	P_MODE[2]	I	misc	H/L	39	AD[30]	I/O	PCI	--
4	TESTI[0]	I	misc	L	40	AD[29]	I/O	PCI	--
5	TESTI[1]	I	misc	L	41	VDD		--	vdd
6	VDD18		--	vdd	42	GND		--	gnd
7	GND		--	gnd	43	AD[28]	I/O	PCI	--
8	AVDD		--	vdd	44	VDD18		--	vdd
9	GND		--	gnd	45	GND		--	gnd
10	AVDD		--	vdd	46	AD[27]	I/O	PCI	--
11	GND		--	gnd	47	GND		--	gnd
12	REXT	O	USB	--	48	AD[26]	I/O	PCI	--
13	RPU_ENA	O	USB	--	49	AD[25]	I/O	PCI	--
14	AVDD		--	vdd	50	AD[24]	I/O	PCI	--
15	GND		--	gnd	51	VDD		--	vdd
16	GND		--	gnd	52	GND		--	gnd
17	FSDP	I/O	USB	--	53	VDD		--	vdd
18	HSDP	I/O	USB	--	54	GND		--	gnd
19	HSDM	I/O	USB	--	55	VDD18		--	vdd
20	FSDM	I/O	USB	--	56	GND		--	gnd
21	GND		--	gnd	57	CBEN[3]	I/O	PCI	--
22	GND		--	gnd	58	IDSEL	I	PCI	--
23	AVDD		--	vdd	59	AD[23]	I/O	PCI	--
24	VDD		--	vdd	60	GND		--	gnd
25	GND		--	gnd	61	AD[22]	I/O	PCI	--
26	VDD18		--	vdd	62	AD[21]	I/O	PCI	--
27	GND		--	gnd	63	AD[20]	I/O	PCI	--
28	TESTI[2]	I	misc	L	64	VDD18		--	vdd
29	TESTI[3]	I	misc	H	65	GND		--	gnd
30	VDD		--	vdd	66	VDD		--	vdd
31	GND		--	gnd	67	GND		--	gnd
32	INTAN	O	PCI	--	68	AD[19]	I/O	PCI	--
33	RSTN	I	PCI	--	69	AD[18]	I/O	PCI	--
34	CLK	I	PCI	--	70	GND		--	gnd
35	GNTN	I	PCI	--	71	AD[17]	I/O	PCI	--
36	REQN	O	PCI	--	72	AD[16]	I/O	PCI	--
73	VDD		--	vdd	109	GND		--	gnd
74	GND		--	gnd	110	AD[7]	I/O	PCI	--
75	CBEN[2]	I/O	PCI	--	111	AD[6]	I/O	PCI	--
76	FRAMEN	I/O	PCI	--	112	AD[5]	I/O	PCI	--
77	GND		--	gnd	113	VDD		--	vdd
78	IRDYN	I/O	PCI	--	114	GND		--	gnd
79	TRDYN	I/O	PCI	--	115	AD[4]	I/O	PCI	--
80	VDD18		--	vdd	116	VDD18		--	vdd
81	GND		--	gnd	117	GND		--	gnd

Pin	Signal name	I/O	Bus	Remarks	Pin	Signal name	I/O	Bus	Remarks
82	DEVSELN	I/O	PCI	--	118	AD[3]	I/O	PCI	--
83	VDD		--	vdd	119	GND		--	gnd
84	GND		--	gnd	120	AD[2]	I/O	PCI	--
85	STOPN	I/O	PCI	--	121	AD[1]	I/O	PCI	--
86	PAR	I/O	PCI	--	122	VDD		--	vdd
87	GND		--	gnd	123	AD[0]	I/O	PCI	--
88	CBEN[1]	I/O	PCI	--	124	GND		--	gnd
89	VDD		--	vdd	125	VDD		--	vdd
90	GND		--	gnd	126	GND		--	gnd
91	VDD18		--	vdd	127	VDD18		--	vdd
92	GND		--	gnd	128	GND		--	gnd
93	AD[15]	I/O	PCI	--	129	CKOUT	O	USB	NC
94	AD[14]	I/O	PCI	--	130	VBDET	I	USB	--
95	VDD		--	vdd	131	misc1	I	misc	L
96	GND		--	gnd	132	misc2	I	misc	L
97	AD[13]	I/O	PCI	--	133	misc3	I/O	misc	NC
98	AD[12]	I/O	PCI	--	134	misc4	I/O	misc	NC
99	GND		--	gnd	135	misc5	I/O	misc	NC
100	VDD18		--	vdd	136	VDD18		--	vdd
101	GND		--	gnd	137	GND		--	gnd
102	AD[11]	I/O	PCI	--	138	misc6	I/O	misc	NC
103	AD[10]	I/O	PCI	--	139	misc7	I/O	misc	NC
104	AD[9]	I/O	PCI	--	140	misc8	O	misc	NC
105	VDD		--	vdd	141	VDD		--	vdd
106	GND		--	gnd	142	XIN	I	USB	--
107	AD[8]	I/O	PCI	--	143	XOUT	O	USB	--
108	CBEN[0]	I/O	PCI	--	144	GND		--	gnd

Note: VDD18 is 1.8V power pins. AVDD and VDD are 3.3V power pins.

6.2. Signal Description

Table 6.2.1 is the description of each pins at PCI mode. Some of the pins are used for difference signals at IHOST mode. Table 6.2.2 is the description of difference signal pins at IHOST mode.

Table 6.2.1 Signal description (PCI mode)

Pin No.	Pin name	I/O	Function
PCI Bus			
38-40,43,46,48-50,59,61-63,68,69,71,72,93,94,97,98,102-104,107,110-112,115,118,120,121,123	AD[31:0] (t/s)	I/O	PCI address data bus.
57,75,88,108	CBEN[3:0] (t/s)	I/O	Bus command byte enable signal.
86	PAR (t/s)	I/O	Even Parity flag.
76	FRAMEN (s/t/s)	I/O	Cycle-frame signal.
79	TRDYN (s/t/s)	I/O	Target RDY signal.
78	IRDYN (s/t/s)	I/O	Initiator RDY signal.
85	STOPN (s/t/s)	I/O	Target termination signal.
82	DEVSELN (s/t/s)	I/O	Device-select signal.
58	IDSEL (in)	I	Device-select signal during configuration.
36	REQN (t/s)	O	PCI bus request signal.
35	GNTN (in)	I	PCI bus grant signal.
34	CLK (in)	I	PCI clock input. Maximum frequency is 33MHz.
33	RSTN (in)	I	PCI bus asynchronous reset input.
32	INTAN (o/d)	O	PCI interrupt signal.
USB			
12	REXT	O	100uA fixed reference bias current pin. Connect to the external resistor with 12.4K Ω .
18	HSDP	I/O	HS_XVR DP pin. To be connected to USB D+ wire.
19	HSDM	I/O	HS_XVR DM pin. To be connected to USB D- wire.
13	RPU_ENA	O	External pull up resistor R _{pu} (1.5k Ω)source drive pin. In high speed operation or disconnect setting, this pin becomes 3-state.
17	FSDP	I/O	FS_XVR DP pin. To be connected to D+ wire via external resistor R _s (39 Ω).
20	FSDM	I/O	FS_XVR DM pin. To be connected to D- wire via external resistor R _s (39 Ω).
142	XIN	I	Connect to external crystal oscillator (48MHz).
143	XOUT	O	Connect to external crystal oscillator (48MHz). If clock oscillator is used, XOUT should be open.
130	VBDET	I	USB Vbus level detect pin. Vbus connects to 15k Ω resistor and this node connects to both VBDET and 30k Ω resistor, which connects to GND.

Pin No.	Pin name	I/O	Function																								
129	CKOUT	O	USB201 IP CKOUT output. This internal clock is monitored for test purpose. At normal operation mode, this pin is fixed to L and should be open.																								
	Misc																										
1-3	P_MODE[2:0]	I	Burst Length select flag. <table border="1"> <thead> <tr> <th>P_MODE[2:0]</th> <th>Burst Length</th> <th>MIN_GNT</th> <th>MAX_LAT</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>32 Bytes</td> <td>2</td> <td>3</td> </tr> <tr> <td>001</td> <td>64 Bytes</td> <td>3</td> <td>6</td> </tr> <tr> <td>010</td> <td>128 Bytes</td> <td>5</td> <td>11</td> </tr> <tr> <td>011</td> <td>256 Bytes</td> <td>9</td> <td>21</td> </tr> <tr> <td>1XX</td> <td>reg setting</td> <td>0</td> <td>0</td> </tr> </tbody> </table> <p>Note: MIN_GNT is calculated based on the latency and MAX_LAT based on 400Mb/s. They take effect on the PCI config header.</p>	P_MODE[2:0]	Burst Length	MIN_GNT	MAX_LAT	000	32 Bytes	2	3	001	64 Bytes	3	6	010	128 Bytes	5	11	011	256 Bytes	9	21	1XX	reg setting	0	0
P_MODE[2:0]	Burst Length	MIN_GNT	MAX_LAT																								
000	32 Bytes	2	3																								
001	64 Bytes	3	6																								
010	128 Bytes	5	11																								
011	256 Bytes	9	21																								
1XX	reg setting	0	0																								
4,5,28,29	TESTI[3:0]	I	LSI shipment test input and mode pin. TESTI[2] should be pulled down. TESTI[1:0] are used to select PCI or IHOST mode. <table border="1"> <thead> <tr> <th>TESTI[1:0]</th> <th>mode</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>PCI</td> </tr> <tr> <td>01</td> <td>IHOST(async)</td> </tr> <tr> <td>10</td> <td>IHOST(sync)</td> </tr> </tbody> </table> <p>TESTI[3] should be pulled up. If TESTI[3] is set to L, TRDY and STOP are not asserted simultaneously during target access with PCI I/F.</p>	TESTI[1:0]	mode	00	PCI	01	IHOST(async)	10	IHOST(sync)																
TESTI[1:0]	mode																										
00	PCI																										
01	IHOST(async)																										
10	IHOST(sync)																										
131,132	Misc[2:1]	I	LSI shipment test pins. Misc[2:1] should be pulled down during normal operation.																								
133-135, 138,139	Misc[7:3]	I/O	LSI shipment test pins. Misc[7:3] should be left open during normal operation.																								
140	Misc[8]	O	LSI shipment test pins. Misc[8] should be left open during normal operation.																								

Table 6.2.2 Signal description (IHOST mode, difference pins from PCI mode)

Pin No.	Pin name	I/O	Function
	IHOST Bus		
72	HREQ_BO1	I/O	The request signal of DMA, BO1. When this signal is asserted, Bulk out data can be read with asserting the HACK_BO1.
71	HACK_BO1	I/O	The acknowledge signal of DMA, BO1. When the HREQ_BO1 signal is asserted, Bulk out data can be read with asserting this signal.
68	LAST_BO1	I/O	This signal indicates the last data of transfer.
69	LBYTE_BO1	I/O	This signal indicates that the only LS byte is valid out of last data word.
63	HREQ_B I2	I/O	The request signal of DMA, B I2. When this signal is asserted, Bulk in data can be written with asserting the HACK_B I2.
62	HACK_B I2	I/O	The acknowledge signal of DMA, B I2. When the HREQ_B I2 signal is asserted, Bulk in data can be written with asserting this signal.
59	LAST_B I2	I/O	This signal indicates the last data of transfer.
61	LBYTE_B I2	I/O	This signal indicates that the only LS byte is valid out of last data word.
50	HREQ_BO3	I/O	Same as HREQ_BO1
49	HACK_BO3	I/O	Same as HACK_BO1
46	LAST_BO3	I/O	Same as LAST_BO1
48	LBYTE_BO3	I/O	Same as LBYTE_BO1

Pin No.	Pin name	I/O	Function
43	HREQ_B I4	I/O	Same as HREQ_B I2
40	HACK_B I4	I/O	Same as HACK_B I2
38	LAST_B I4	I/O	Same as LAST_B I2
39	LBYTE_B I4	I/O	Same as LBYTE_B I2
93,94,97, 98, 102-104, 107, 110-112, 115,118, 120,121, 123	HDAT[15:0]		IHOST data bus.
57,75,85, 86,88, 108	HADR[5:0]	I/O	IHOST address signal.
76	HWRN	I/O	IHOST write strobe signal.
78	HRDN	I/O	IHOST read strobe signal.
58	HCSN	I	IHOST chip select signal.
36	HRDY	O	IHOST ready signal.
34	CLK	I	PCI clock input. Maximum frequency is 33MHz. Same as PCI mode.
33	RSTN	I	PCI bus asynchronous reset input. Same as PCI mode.
32	HIRQ	O	IHOST interrupt signal.

7. Overview of Operation

7.1. Reset

7.1.1. Hard reset

Immediately after powering up, input a reset signal from the PCI to the RSTN pin to initialize the device.

All logic in the device is initialized, as well as the configuration register.

7.1.2. Soft reset

Execute a soft reset by setting the internal registers. There are two major types of soft reset: U2P control soft reset and HS_SIE soft reset.

7.2. Overview of U2P control operation (descriptor mode)

Device has DMAC_D(descriptor) mode, DMAC_P(page) mode and IHOST mode for data transfer. After setting required information in each register, activate DMAC to start the transfer.

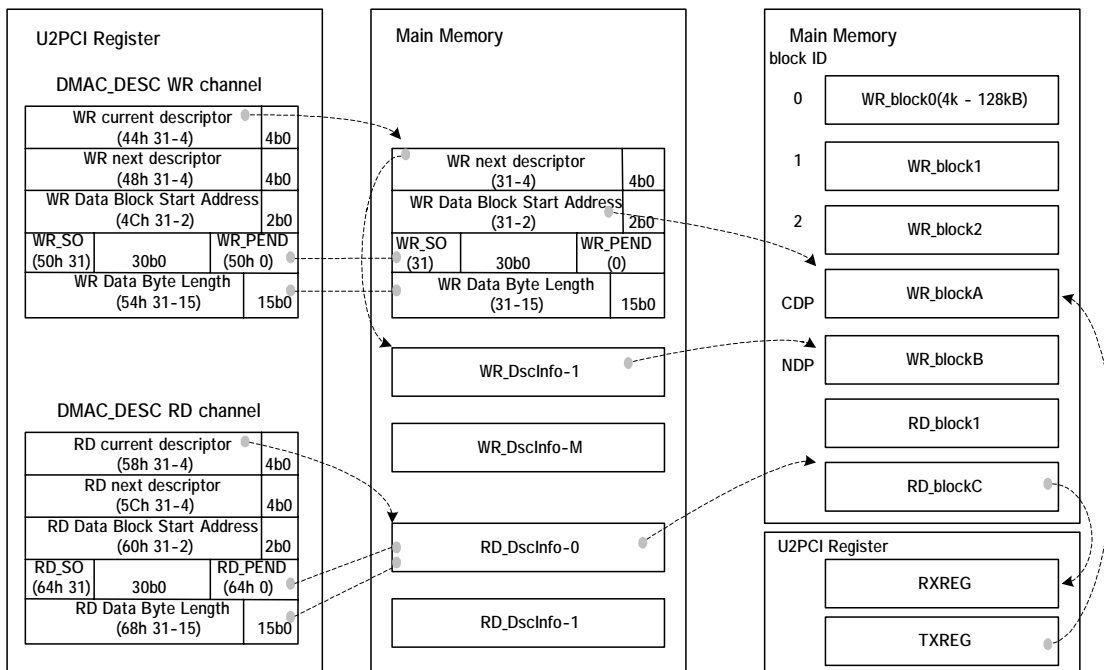
In DMAC_D mode, external descriptor is used to control. The device reads the descriptor information at the address set in the register. If the SO flag is 0, the device accesses the data at the address indicated by the pointer. When a block of data has been transferred, the device accesses the next pointed address space.

If the SO flag is 1, the device stops transfer and polls the flag at a regular interval. When the SO flag becomes 0, the device restarts the access.

In DMAC_P mode the control sequence is same as DMAC_D mode. The difference is that the sequence is controlled by using internal register.

Figure 7.2 shows the correspondence of descriptors.

Figure 7.2 Correspondence of descriptors



7.3. Overview of HS_SIE operation

This block connected to USB201IP, HS_SIE controls the USB bus. It has two 512-byte buffers that are used for buffering USB data and data transfer with DBUF.

It also performs basic level USB operation, basic transaction flow control, HS chirp protocol and HS/FS judgement.

7.4. IHOST interface

IHOST interface has a simple transaction with a few control signals. HCSN, HWRN, HRDN and HRDY are used for register access. Asserting the HCSN and HWRN with setting the HADR and HDAT, CPU can write data to internal registers. Device will assert HRDY to indicate the transaction is completed. In read operation, CPU must assert HRDN. Device will assert HRDY when data is ready.

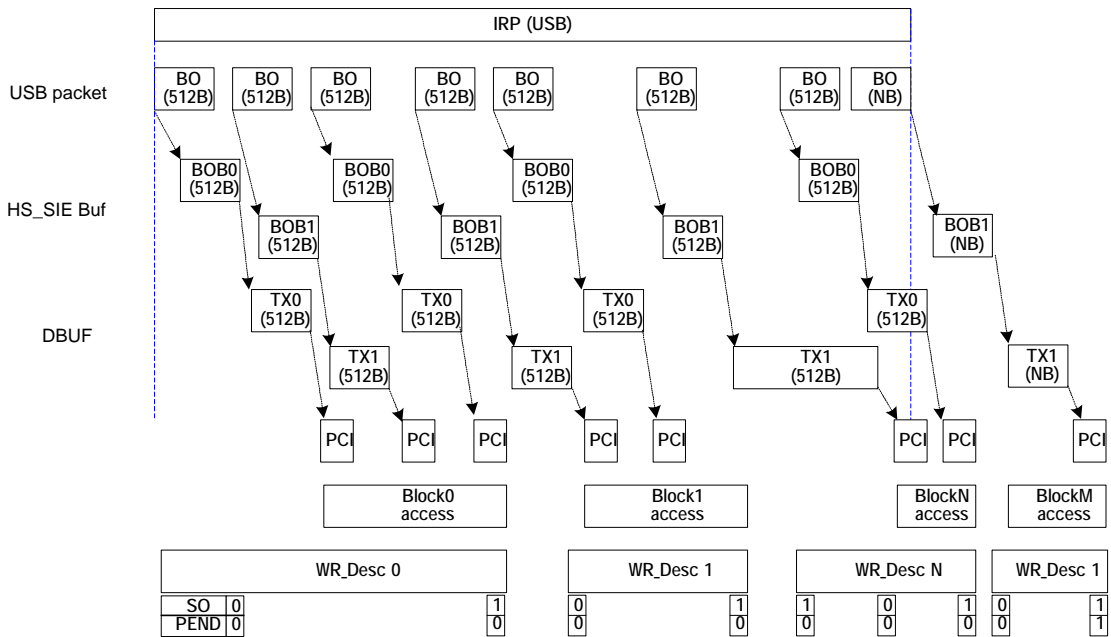
HREQ and HACK are used for DMA. Device asserts HREQ when it's ready for data access. CPU can access with asserting HACK.

8. Operation Timing

The following chart shows the operation timing for Bulk Out transfer.

PEND is the flag indicating the end of transfer. SO flag tells changing the descriptor and PEND tells the end of transfer.

Figure 8 Bulk Out operation timing



9. References

- a. PCI Specification Rev. 2.2 by PCI SIG
- b. USB Specification Rev. 2.0 by USB IF
- c. KL5KUSB200 – USB2.0 Compliant Transceiver Chip Datasheet Rev 0.2 by Kawasaki Microelectronics, Inc..
- d. KL5BUDV002 datasheet
- e. KL5BUDV003 datasheet

KL5BUDV003 Information sheet

Rev. 0.1 8/20/2002

IHOST timing information

IHOST bus IF has 16bits bus with register access and 4-channel DMA.
 The register access mode needs only HCSN, HWRN, HRDN and HRDY for control.

DMA access is controlled with HREQ and HACK signal. Each 4-channel DMA has independent control signals.

Followings are the timing diagram of IHOST IF.

Figure 1 IHOST timing (1)
 Register write timing

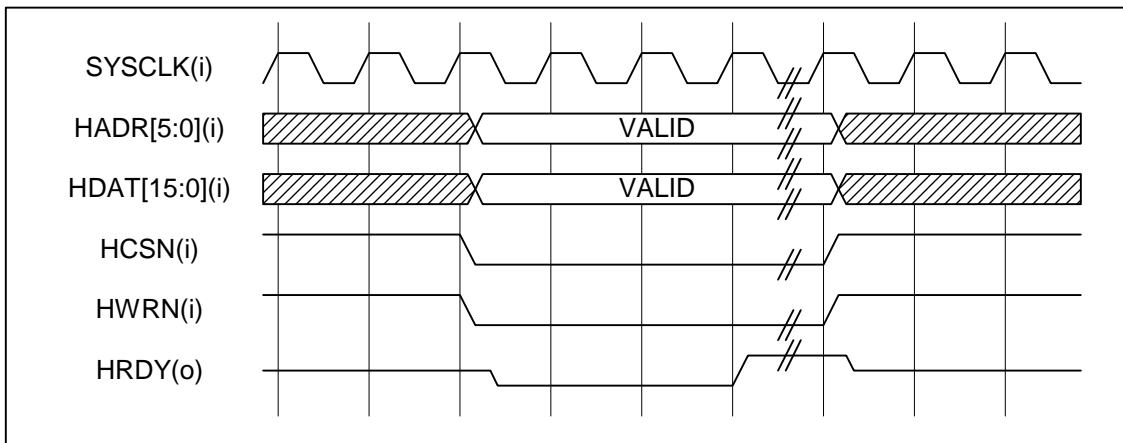


Figure 2 IHOST timing (2)
 Register read timing

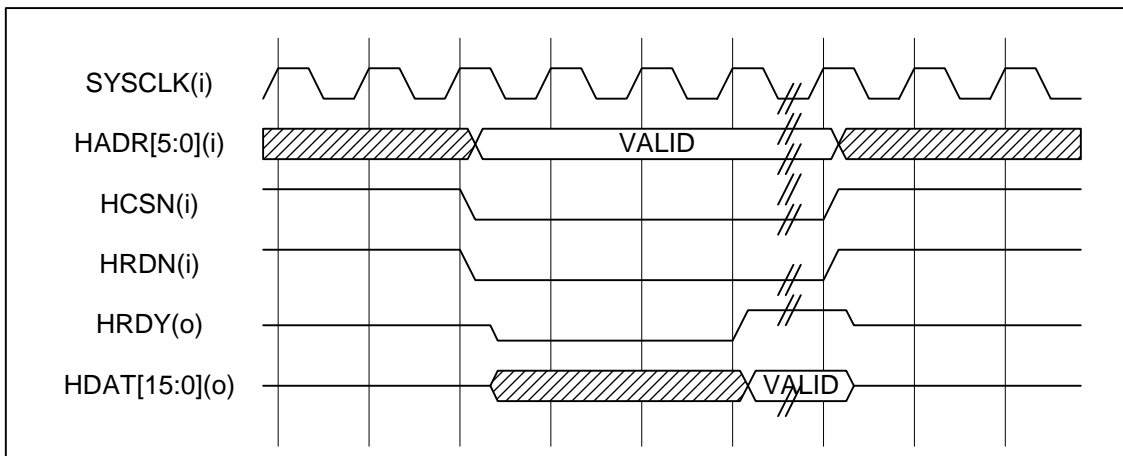


Figure 3 IHOST timing (3)
DMA read timing

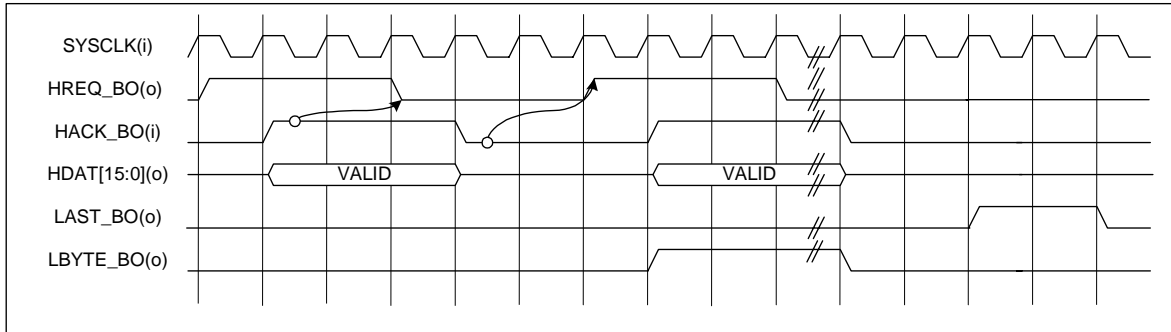


Figure 4 IHOST timing (4)
DMA write timing

